wherein the gate region is characterized as a trench having a bottom and sidewalls, the gate dielectric overlies the bottom of the trench, the inner spacer layer is in contact with the sidewalls of the trench, and the silicide structure fills the trench.

[c16] A semiconductor device according to claim ~~16~~ 15, wherein the inner spacer layer overlies the gate dielectric and is in contact therewith.

[c17] A semiconductor device according to claim 15, wherein the gate region has disposed therein a first silicide structure and a second silicide structure, and a portion of said inner spacer layer separates the first silicide structure and the second silicide structure.

[c18] A semiconductor device according to claim 17, further comprising a metal layer overlying the first silicide structure and the second silicide structure and in contact therewith.

[c19] A semiconductor device according to claim 15, wherein the inner spacer layer comprises
silicon nitride.

[c20] A semiconductor device according to claim 17, wherein the gate region includes a first portion and a second portion, the first portion having disposed therein a first